

Adjusted Patent Claims (Post-Prior-Art)

PT-NPU — Parallel Temporal-Logic Neuromorphic Processing Unit

คำอธิบายการปรับปรุง: หลังจากค้นหา Prior Art พบว่ามี 3 องค์ประกอบที่ novelty สูงมาก (PIF, Security, Dual-Mode) และ 2 องค์ประกอบที่มี prior art บางส่วน (3D Crossbar, AER) จึงปรับภาษา Claims ให้: - **กว้างขึ้น** สำหรับองค์ประกอบที่ไม่มี prior art (PIF, Security) - **แคบลง** (add specific limitations) สำหรับองค์ประกอบที่มี prior art บางส่วน

CLAIM 1 (Independent — Hardware Architecture) — ปรับภาษาให้แข็งแรงขึ้น

~~A neuromorphic processing architecture comprising:~~

Neuromorphic processing apparatus comprising a monolithic integrated circuit, the apparatus comprising:

- a. a CMOS base layer monolithically fabricated on a silicon substrate, said CMOS base layer comprising a plurality of mixed-signal Complementary Metal-Oxide-Semiconductor (CMOS) circuits configured as Predictive Integrate-and-Fire (PIF) neurons arranged in an array, wherein each said PIF neuron comprises a first differentiator circuit configured to compute a first temporal derivative dV/dt of a membrane potential and a second differentiator circuit configured to compute a second temporal derivative d^2V/dt^2 of said membrane potential;

- b. a plurality of memristive layers monolithically integrated directly above and in physical contact with said CMOS base layer using Back-End-Of-Line (BEOL) processing without an intervening semiconductor substrate, said memristive layers comprising a three-dimensional (3D) crossbar array of 1T1R (one transistor, one resistor) memristor cells configured as hardware synapses, each said memristor cell storing a non-volatile analog conductance representing a synaptic weight, wherein said memristor cells are configured to perform analog matrix-vector multiplication via Kirchhoff's Current Law summation along bitlines; and
- c. an asynchronous routing network embedded in said CMOS base layer, said routing network employing Address Event Representation (AER) protocol to transmit spike packets between said PIF neurons, wherein each router node in said routing network comprises a power-gating switch configured to disconnect power during idle periods and to restore power within 1 nanosecond upon arrival of a spike packet;

wherein said apparatus performs neural network inference operations without accessing off-chip memory.

CLAIM 2 (Dependent — PIF Pre-emptive Firing) — คงเดิม (novelty สูง)

The apparatus of claim 1, wherein each said PIF neuron further comprises a Predictive Fire Logic (PFL) circuit configured to compute a predicted membrane potential V_{pred} at a future time according to:

$$V_{pred} = V_{mem} + \alpha \cdot dV/dt + \beta \cdot d^2V/dt^2 + \gamma \cdot \int I_{in} dt$$

where V_{mem} is instantaneous membrane potential, dV/dt is the first temporal derivative output of said first differentiator circuit, d^2V/dt^2 is the second temporal derivative output of said second differentiator circuit, $\int I_{in} dt$ is an integrated input current, and α , β , γ are programmable coefficients stored in on-chip registers; and wherein said PFL is further configured to generate a pre-emptive spike when said V_{pred} equals or exceeds a threshold voltage $V_{threshold}$ before said V_{mem} reaches said $V_{threshold}$.

CLAIM 3 (Dependent — Adaptive Prediction Window) — คงเดิม

The apparatus of claim 2, wherein said PFL is further configured to compute an adaptive prediction window Δt_{pred} according to:

$$\Delta t_{\text{pred}} = (V_{\text{threshold}} - V_{\text{mem}}) / (|dV/dt| + \epsilon)$$

where ϵ is a positive constant, and wherein said pre-emptive spike is generated at a time $t_{\text{pred}} = t_{\text{fire}} - \Delta t_{\text{pred}}$, where t_{fire} is a time at which V_{mem} would reach $V_{\text{threshold}}$ in a conventional integrate-and-fire mechanism operating on said V_{mem} without said first derivative and said second derivative.

CLAIM 4 (Dependent — Dual Firing Mode) — คงเดิม (novelty สูง)

The apparatus of claim 1, wherein each said PIF neuron is configured with a dual-mode firing logic comprising:

- a. a predictive mode generating said pre-emptive spike when said $V_{\text{pred}} \geq V_{\text{threshold}}$, irrespective of whether said V_{mem} has reached said $V_{\text{threshold}}$; and
- b. a reactive mode generating a normal spike when said $V_{\text{mem}} \geq V_{\text{threshold}}$ and said $V_{\text{pred}} < V_{\text{threshold}}$;

wherein said dual-mode firing logic switches between said predictive mode and said reactive mode on a per-spike basis in real-time without interrupting neural computation, and wherein said reactive mode serves as a fallback mechanism when said predicted membrane potential V_{pred} is unavailable or unreliable.

CLAIM 5 (Dependent — 3D Crossbar Stacking) — ปรับ ให้แคบลง เพิ่ม specific limitations

~~The architecture of claim 1, wherein said at least one memristive layer comprises 4 to 16 stacked crossbar layers...~~

The apparatus of claim 1, wherein said plurality of memristive layers comprises at least four vertically stacked crossbar layers fabricated monolithically above said CMOS base layer using only Back-End-Of-Line (BEOL) processing, each said crossbar layer comprising wordlines and bitlines arranged orthogonally, a 1T1R (one transistor, one resistor) memristor cell at each crosspoint wherein said access transistor is disposed in said CMOS base layer, and an Inter-Layer Dielectric (ILD) layer of thickness 50-100 nm separating adjacent crossbar layers, connected by conductive vertical via arrays.

CLAIM 6 (Dependent — STDP Online Learning) — คงเดิม (prior art มี แต่เป็น dependent)

The apparatus of claim 1, further comprising a Spike-Timing-Dependent Plasticity (STDP) circuit monolithically integrated in said CMOS base layer, said STDP circuit configured to detect a temporal difference Δt between a pre-synaptic spike arrival time and a post-synaptic spike generation time, and responsive to said Δt , to apply a SET voltage pulse across a selected memristor cell in said 3D crossbar array when said Δt indicates potentiation or a RESET voltage pulse when said Δt indicates depression, thereby updating said non-volatile analog conductance in real-time without software intervention.

CLAIM 7 (Dependent — AER Power Gating) — ปรับให้เฉพาะเจาะจงมากขึ้น (แยกจาก Loihi)

The apparatus of claim 1, wherein said asynchronous routing network comprises:

- a. an AER encoder disposed in said CMOS base layer and configured to generate an address packet comprising at least a source neuron identifier, a timestamp, and a priority flag upon each spike event output by a PIF neuron;
- b. a router node disposed in said CMOS base layer and comprising an arbiter for collision resolution using a 4-phase bundled-data handshake protocol, and an asynchronous FIFO buffer; and

- c. a power-gating switch comprising a PMOS header transistor or NMOS footer transistor configured to disconnect a supply voltage from said router node during an idle state when no spike packets are present, and to reconnect said supply voltage within 1 nanosecond upon arrival of a request signal from any input port of said router node;

wherein said idle state consumes leakage current of less than 1 picoampere per router node.

CLAIM 8 (Independent — PIF Method) — คงเดิม

A method for predictive integrate-and-fire processing in a neuromorphic circuit, comprising:

- a. integrating an input current from a memristive crossbar array in a current integrator to produce a membrane potential V_{mem} ;
 - b. computing a first derivative dV/dt of said membrane potential via a first analog differentiator circuit and computing a second derivative d^2V/dt^2 of said membrane potential via a second analog differentiator circuit, said computing performed simultaneously with said integrating;
 - c. computing a predicted membrane potential V_{pred} at a future time using said V_{mem} , said dV/dt , said d^2V/dt^2 , and an integrated history term;
 - d. comparing said V_{pred} against a threshold $V_{\text{threshold}}$ using a first comparator;
 - e. if said $V_{\text{pred}} \geq \text{said } V_{\text{threshold}}$, generating a pre-emptive spike and resetting said membrane potential to a reset value; and
 - f. if said $V_{\text{pred}} < \text{said } V_{\text{threshold}}$ and said $V_{\text{mem}} \geq \text{said } V_{\text{threshold}}$, generating a normal spike and resetting said membrane potential to said reset value.
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CLAIM 9 (Dependent — Decoupled Sampling) — คงเดิม

The method of claim 8, wherein steps (c) through (e) are performed on values of V_{mem} , dV/dt , and d^2V/dt^2 synchronously sampled via a sample-and-hold circuit at discrete sampling intervals Δt_{sample} of 100 picoseconds to 1 nanosecond, such that said prediction computation in step (c) does not interfere with said integration of step (a).

CLAIM 10 (Independent — Hardware Security) — คงเดิม (novelty สูง)

A hardware security system for a neuromorphic integrated circuit, comprising:

- a. at least one decoy spike generator configured to generate decoy electrical spikes having electrical characteristics indistinguishable from genuine neural spikes, said decoy spikes containing no data payload;
 - b. an obfuscated routing path controlled by a Physical Unclonable Function (PUF) circuit, said PUF providing a chip-unique identifier used as a seed to randomize address packet routing within an asynchronous routing network;
 - c. a power profile randomizer comprising a current-steering digital-to-analog converter (DAC) configured to inject pseudo-random alternating current (AC) noise into a power distribution network at frequencies between 100 megahertz and 10 gigahertz, masking power signatures of genuine neural computation; and
 - d. an anti-tamper mesh comprising a fine-pitch wire mesh of line width less than 100 nanometers disposed at a topmost metal layer of said integrated circuit, a continuity monitoring circuit configured to detect an open circuit condition in said anti-tamper mesh, and an erase circuit responsive to said continuity monitoring circuit configured to switch all memristor cells in a memristive crossbar array to a high-resistance state within 100 nanoseconds upon detection of said open circuit condition.
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CLAIM 11 (Dependent — Decoy Priority) — ปรับให้ชัดเจนขึ้น

The system of claim 10, wherein said decoy spike generator comprises a pseudo-random number generator driving multiple decoy spike generators distributed across said integrated circuit, and wherein said decoy spikes are assigned a lowest priority value in a priority field of AER address packets, such that said decoy spikes are routed only when no genuine spikes of higher priority are pending, thereby preventing said decoy spikes from delaying routing of said genuine neural spikes.

CLAIM 12 (Dependent — Fabrication Method) — ปรับให้อ้างอิง specific materials

A method for fabricating the apparatus of claim 1, comprising:

- a. fabricating said CMOS base layer on a silicon wafer using a CMOS process at a technology node of 28 nanometers or smaller, said CMOS base layer containing said PIF neurons, said AER routing network, said STDP circuit, and said hardware security system;
- b. planarizing a top surface of said CMOS base layer using Chemical Mechanical Polishing (CMP);
- c. fabricating a first memristive crossbar layer above said CMOS base layer using BEOL processing, comprising: depositing a bottom electrode comprising titanium nitride (TiN) or tantalum nitride (Ta₂N₅) to a thickness of 10-20 nanometers, depositing a metal-oxide switching layer comprising hafnium dioxide (HfO₂) or tantalum oxide (Ta₂O₅) to a thickness of 5-10 nanometers, depositing a top electrode comprising titanium nitride/platinum (TiN/Pt) or titanium nitride/titanium (TiN/Ti) to a total thickness of 10-20 nanometers, and etching to define individual 1T1R memristor cells;
- d. depositing an Inter-Layer Dielectric of silicon dioxide (SiO₂) or low-k dielectric;
- e. repeating steps (c) and (d) for each additional memristive crossbar layer up to a total of at least four layers; and

- f. fabricating a micro-cooling layer comprising embedded microfluidic channels, an electromagnetic shielding layer, and an anti-tamper continuity mesh at a topmost metal layer.
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**CLAIM 13 (Dependent — Non-Volatile Instant-On) —
เพิ่มเติม (utility)**

The apparatus of claim 1, wherein said non-volatile analog conductances stored in said memristor cells persist without electrical power, enabling the apparatus to begin neural network inference within 1 microsecond of power application without loading synaptic weights from any external memory.

**CLAIM 14 (Dependent — Multi-Energy Domain) — ปรับ
ใหม่**

The apparatus of claim 1, further comprising a low-power mode controller configured to reduce a number of active memristive crossbar layers or to reduce a bit resolution of said programmable coefficients α , β , γ from 8 bits to 4 bits, thereby reducing power consumption at a cost of reduced prediction accuracy.

**CLAIM 15 (Independent — Multi-Temporal Processing
Method) — คงเดิม**

A method of multi-temporal signal processing in a neuromorphic architecture, comprising:

- a. decomposing an input signal into overlapping temporal frames using an asynchronous shift register;
- b. processing said temporal frames in parallel across a plurality of interconnected PIF neurons via said asynchronous AER routing network;
- c. integrating predictions from said temporal frames using a time-warped integration mechanism wherein a pre-emptive spike generated from a future temporal frame immediately influences integration of a present temporal frame; and

- d. generating an output spike encoding information from multiple temporal frames simultaneously.

CLAIM 16 (New — Differentiator-Based PIF Circuit)

เพิ่มเพื่อป้องกัน competitor เลี่ยง Claim 1 โดยอ้างว่าทำเป็น software แทน hardware

A Predictive Integrate-and-Fire (PIF) neuron circuit, comprising:

a current integrator configured to produce a membrane potential V_{mem} from an input current;

a first analog differentiator circuit operatively coupled to said current integrator and configured to compute a first derivative dV/dt of said membrane potential;

a second analog differentiator circuit operatively coupled to said first analog differentiator circuit and configured to compute a second derivative d^2V/dt^2 of said membrane potential;

a Predictive Fire Logic circuit operatively coupled to said current integrator, said first analog differentiator circuit, and said second analog differentiator circuit, said Predictive Fire Logic circuit configured to compute:

$$V_{\text{pred}} = V_{\text{mem}} + \alpha \cdot dV/dt + \beta \cdot d^2V/dt^2 + \gamma \cdot I_{\text{in}} \, dt$$

and to generate a pre-emptive spike when $V_{\text{pred}} \geq V_{\text{threshold}}$;

wherein said first analog differentiator circuit, said second analog differentiator circuit, and said Predictive Fire Logic circuit are configured to operate simultaneously and in parallel with said current integrator.

CLAIM 17 (New — Decoy Spike Statistical Matching)

เพิ่ม Specificity ให้ Security Claim

The system of claim 10, wherein said decoy spike generator is configured to generate decoy spike trains whose statistical inter-spike interval distribution matches a Poisson distribution or a gamma distribution of genuine neural spike activity in said

neuromorphic integrated circuit, thereby rendering said decoy spikes statistically indistinguishable from genuine spikes under oscilloscope observation, logic analyzer capture, or power trace analysis using differential power analysis (DPA) or simple power analysis (SPA).

CLAIM 18 (New — Energy Monitoring Based on Prediction)

The apparatus of claim 1, further comprising an energy monitoring circuit configured to measure a rate of pre-emptive spikes generated by said PIF neurons versus a rate of normal spikes, and responsive to said measurement, to adjust said programmable coefficients α , β , γ to optimize energy efficiency for a given input pattern.

สรุปจำนวน Claims

Claim #	Type	Scope	Novelty Level
1	Independent	Hardware Architecture	★★★
2	Dependent	PIF Equation	★★★
3	Dependent	Adaptive Window	★★★
4	Dependent	Dual-Mode	★★★
5	Dependent	3D Crossbar	★★☆
6	Dependent	STDP	★★☆
7	Dependent	AER Power Gating	★★☆
8	Independent	PIF Method	★★★
9	Dependent	Decoupled Sampling	★★★
10	Independent	Security System	★★★
11	Dependent	Decoy Priority	★★★
12	Dependent	Fabrication	★★☆
13	Dependent	Instant-On	★★☆
14	Dependent	Multi-Energy	★★☆

Claim #	Type	Scope	Novelty Level
15	Independent	Multi-Temporal	★★★
16	Independent	PIF Circuit (specific)	★★★
17	Dependent	Decoy Statistics	★★★
18	Dependent	Energy Optimization	★★★